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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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2-25-03

In re Patent Application of:

Michael Powell, et al.

Application No.: 08/887,680

Filed: July 3, 1997

For: METHOD AND APPARATUS FOR
EXTENDING COMPUTER ARCHITECTURE
FROM 32 TO 64 BITS

) Examiner: David Y. Eng

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) Art Unit: 2155

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Assistant Commissioner for Patents
Washington, D.C. 20231

Technology Center 2100

SUPPLEMENTAL APPEAL BRIEF

Appellants submit, in triplicate, the following Supplemental Appeal Brief pursuant to 37 C.F.R. § 1.193(b)(2) and respectfully request reinstatement of an appeal that was the subject of Appellants' Appeal Brief filed on February 27, 2001. This Supplemental Appeal Brief is being filed following the re-opening of prosecution in a non-final Office Action dated October 16, 2002. In the October 2002 Office Action, the Examiner withdrew his indication that the application was in condition for allowance and that prosecution as to the merits was closed, as previously set forth in an *Ex parte Quayle* action dated May 21, 2001. The *Ex parte Quayle* action was issued by the Examiner in response to Appellants' Appeal Brief of February 27, 2001.

Pursuant to 37 C.F.R. § 1.193(b)(2) and MPEP § 1208.02, Appellants do not submit a fee in connection with this Supplemental Appeal Brief since the fee has been previously paid. Please charge any additional amount due or credit any overpayment to Deposit Account 02-2666.

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I. REAL PARTY IN INTEREST

Michael Powell, the party named in the caption, Robert Cmelik, Shing Kong, David Ditzel, and Edmund Kelly transferred their rights to that which is disclosed in the subject application through an assignment recorded on December 21, 1990 (5555/0186) to Sun Microsystems, Inc. of Mountain View, California. Thus, as the owner at the time the brief is being filed, Sun Microsystems, Inc. of Mountain View, California is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences that will affect or be affected by the outcome of this appeal.

III. STATUS OF CLAIMS

Claims 1-38 are pending in this application. Claims 1-16 are allowed. Claims 17-38 stand rejected and are presented for appeal. The Appendix contains the claims as currently pending.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed September 27, 2000.

V. SUMMARY

Pursuant to MPEP § 1208.02, Appellants hereby incorporate by reference from Appellants' Appeal Brief filed February 27, 2001, the section entitled "Summary of the Invention."

VI. ISSUES

The issue involved in this appeal is as follows:

Are Claims 17-38 unpatentable under 35 U.S.C. § 251 as being an improper recapture of subject matter surrendered in the application for the patent upon which the present reissue is based?

VII. GROUPING OF CLAIMS

Appellants submit that the claims do not stand or fall together. Accordingly, Appellants group the claims as follows:

Group I	Claims 17-32
Group II	Claims 33-38

The reason for the independent patentability of the separate groups is discussed in detail below.

VIII. ARGUMENT

Rejection of Claims 17-38 Based on Improper Recapture

The Examiner argues that during prosecution of the parent application, Appellants relied upon certain limitations to show patentability over the cited references (Preliminary Amendment, filed October 11, 1994, Application No. 08/321,459, U.S. Patent No. 5,430,864). Specifically, the Examiner points to “a most significant bit of the stack pointer register,” “the most significant bit of the stack pointer register indicates the first word size,” “setting a width indication bit in the first stack save area in memory,” and “the width indication bit in the first stack save area in memory indicates that the data values for the procedure have the second word size.” These limitations will be addressed in turn based on their relevance to Groups I and II.

A. Group I: “Most Significant Bit”

The Examiner rejects the claims of Group I under 35 U.S.C. § 251 as being an improper recapture of subject matter surrendered in the parent application. The Examiner states that the limitations “a most significant bit of the stack pointer register” and “the most significant bit of the stack pointer register indicates the first word size” were added to Claims 73 and 81 (which issued

as Claims 1 and 9) in order to overcome a rejection and to procure issuance of the parent application. Presumably, the Examiner concludes that the absence of a “most” significant bit in the rejected claims amounts to recapture of subject matter surrendered by Appellants. However, Appellants disagree with the Examiner’s conclusion.

Under MPEP § 1412.02, a patentee is free to acquire, through reissue, claims that are narrower in scope in all aspects than claims canceled from the original application to obtain a patent (emphasis added). However, if the reissue claims are narrower than the claims canceled from the original application, yet broader than the original patent claims, reissue must be sought within two years after the grant of the original patent (emphasis added).

In re Clement, 131 F.3d 1464, 45 U.S.P.Q.2d 1161 (Fed. Cir. 1997), is the case that MPEP § 1412.02 relies on to set forth the two step test for the recapture rule. A closer look at Clement shows support for the proposition that reissue claims that are narrower than the canceled claims yet broader than the patent claims should be allowable. Specifically, Clement states that “[i]f the scope of the reissue claim is the same as or broader than that of the canceled claim, then the patentee is clearly attempting to recapture surrendered subject matter and the reissue claim is, therefore, unallowable. In contrast, a reissue claim narrower in scope [than the canceled claim] escapes the recapture rule entirely.” (emphasis added). Id. at 1469.

Here, the claims of Group I are narrower than the canceled claims and should not be subject to the recapture rule. In this regard, Appellants first note that canceled Claims 55-72 of the parent application recited “testing an indication bit.” The Examiner previously stated in the Final Office Action dated September 27, 2000, that canceled Claims 55-72 of the parent application did not require any specific bit to be the indication bit, and thus, any bit could be used as the indication bit (emphasis added). However, the claims of Group I recite, among other limitations, only testing the least significant bit.

Given the Examiner’s interpretation of “an indication bit,” specifically reciting a least significant bit is narrower than reciting “an indication bit,” as set forth in canceled Claims 55-72 of the parent application. In addition to the narrowing recitation of a “least significant bit,” only a

brief review is necessary to see that independent Claims 17 and 25 are narrower in scope in all aspects than canceled independent Claims 55 and 64.

Accordingly, Appellants do not impermissibly recapture that which was given up by canceling Claims 55-72 of the parent application (e.g., ability to test any bit). Rather, Appellants have submitted reissue claims that are narrower in scope in all aspects than those that were canceled. Although the scope of the reissue claims relative to the scope of the issued patent claims is not an issue, Appellants note that the reissue application was filed on July 3, 1997, which was within two years after the grant of the original patent on July 4, 1995. Thus, it is permissible for Appellants' reissue claims to be broader than the issued patent claims.

In light of the foregoing, Appellants respectfully request that the rejection of the claims of Group I be overturned.

B. Group II: "Most Significant Bit" and "Width Indication Bit"

The Examiner rejects the claims of Group II under 35 U.S.C. § 251 as being an improper recapture of subject matter surrendered in the parent application for the same reasons as Group I. In addition, the Examiner states that the limitations "setting a width indication bit in the first stack save area in memory," and "the width indication bit in the first stack save area in memory indicates that the data values for the procedure have the second word size" were added to Claim 73 (which issued as Claim 1) in order to overcome a rejection and to procure issuance of the parent application. The Examiner concludes that the limitations directed towards a width indication bit cannot be omitted from reissue Claim 33. However, Appellants disagree with the Examiner's conclusion.

Appellants first note that the reasoning and arguments set forth above regarding the absence of limitations directed toward a "most" significant bit apply equally to the claims of Group II.

As mentioned above, MPEP § 1412.02 sets forth the two step test for the recapture rule described in Clement. The first step of the test is to determine whether and in what aspect the

reissue claims are broader than the patent claims. In this regard, a reissue claim is broadened where some limitation of the patent claims is no longer required in the reissue claim.

The second step is to determine whether the broader aspects of the reissue claims relate to surrendered subject matter. An omitted or broadened limitation relates to surrendered subject matter if the limitation was originally presented/argued/stated in the original application to make the claims allowable over a rejection or objection made in the original application. MPEP § 1412.02 gives three examples of situations that indicate that a limitation relates to surrendered subject matter: (1) an argument, specific as to the limitation, that the claim limitation defined over the rejection (emphasis added); (2) adding a limitation for the purpose of making the claims allowable over a rejection or objection; and (3) the Examiner's Reasons for Allowance state that a specific limitation was responsible for distinguishing over a potential combination of references.

Regarding the first step of the test for recapture, the limitation "a width indication bit in the first stack save area in memory" is absent from the claims of Group II. Thus, the claims of Group II are broader than the patent claims in this regard (e.g., omission of "a width indication bit in the first stack save area in memory").

Turning to the second step, one must ascertain whether the omitted limitation relates to surrendered subject matter. Appellants will discuss, in turn, the relevant amendments, arguments, and Examiner's Reasons for Allowance in the prosecution history.

Regarding the amendments, a closer review of Claims 55-72 of the parent application shows that independent Claims 55 and 64 of the parent application both include a limitation analogous to "setting the width indication bit." Specifically, Claims 55 and 64 of the parent application included limitations directed to "setting an indication bit corresponding to said procedure in said stack save area" (Claim 55, line 12; Claim 64, lines 12 and 13). This is analogous to "setting a width indication bit in the first stack save area" since both the "indication bit" of Claims 55 and 64 of the parent application and the "width indication bit" of Claims 73-88 of the parent application indicate whether the data being saved is of a first word size or a second word size. Thus, "setting a width indication bit" was not added in order to obtain the patent upon which

the present reissue is based. Rather, the limitation was already present in an analogous form and was merely reworded in Claims 73-88.

Moreover, in the Advisory Action dated September 24, 1994, Examiner Phillip refused to enter an amendment (e.g., adding new Claims 73-88 of the parent application) because “testing a most significant bit of a stack pointer is a new limitation that would require further consideration and/or search.” Absent from the Advisory Action is any characterization of the step of “setting the width indication bit” as a new limitation that would require further consideration and/or search. Thus, Examiner Phillip did not view “setting a width indication bit” as a new limitation.

Accordingly, the prosecution history shows that no amendments were made such that the “width indication bit” of the issued patent claims can be properly characterized as “relating to surrendered subject matter.”

Regarding arguments in the prosecution history, when Claims 73-88 were added, no arguments were made to specifically indicate that the width indication bit distinguished Appellants’ claims from the cited art. Rather, the arguments for patentability were specifically directed towards the use of the most significant bit of a stack pointer register to indicate word size (Preliminary Amendment filed October 11, 1994, page 9, lines 19 and 20; page 11, lines 10-12; page 11, line 25-page 12, line 2). Thus, no arguments, specific to the “width indication bit,” were made in order to define over the rejections.

Finally, the Notice of Allowability indicates that “[t]he art of record fails to teach, remotely suggest, or render obvious storing an indication of word size in the most significant bit of the stack pointer register or means for performing the recited function(s)” (page 1, numbered paragraph 5). However, no statements were made to indicate that the limitation directed towards a “width indication bit” distinguished over the art of record.

In light of the foregoing, the amendments, arguments, and Examiner’s statement regarding the allowability of the claims in the prosecution history clearly shows that the limitation of a “width indication bit” is not related to the surrendered subject matter. Thus, the second requirement of the test for recapture is not satisfied. Accordingly, the absence of the step of “setting a width

“indication bit” in Appellants’ reissue claims does not constitute an impermissible recapture of surrendered subject matter.

Under MPEP § 1412.02, reissue claims that are broader in certain aspects and narrower in others *vis-à-vis* claims canceled from the original application to obtain a patent may avoid the effect of the recapture rule if the claims are broader in a way that does not attempt to reclaim what was surrendered earlier. As discussed above, the claims of Group II are broader (e.g., absence of “width indication bit”) in a manner that does not attempt to reclaim surrendered matter. The claims of Group II are also narrower than the canceled claims since the claims of Group II recite a “least significant bit” rather than “an indication bit,” as recited in the canceled claims. However, the merits and effects of such a narrowing have been discussed above and do not preclude the allowability of the claims of Group II.

Accordingly, Appellants respectfully request that the rejection of the claims of Group II be overturned.

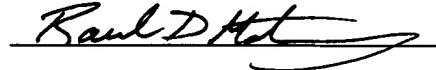
IX. CONCLUSION AND RELIEF

Based on the foregoing, Appellants request that the Board overturn the remaining rejections and hold that all of the claims of the present application are allowable.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 2/11/03

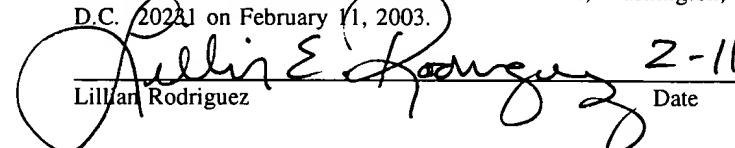


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Lillian Rodriguez

2-11-03
Date

X. APPENDIX

The claims involved in this Appeal are as follows:

1 1. A method for context switching a processor that executes procedures having
2 differing word sizes, comprising the steps of:

3 testing a most significant bit of a stack pointer register in the processor that indicates
4 whether a set of data values for a procedure that are stored in a set of registers in the processor
5 each have a first word size or a second word size wherein the first word size is less than the
6 second word size;

7 transferring the data values from a least significant portion of each register to a first stack
8 save area in memory and transferring a least significant portion of a stack pointer value from the
9 stack pointer register to the first stack save area in memory if the most significant bit of the stack
10 pointer register indicates the first word size;

11 setting a width indication bit in the first stack save area in memory, and transferring the data
12 values from the registers to a second stack save area in memory and transferring the stack pointer
13 value from the stack pointer register to the second stack save area if the most significant bit of the
14 stack pointer register indicates the second word size such that the width indication bit in the first
15 stack save area in memory indicates that the data values for the procedure have the second word
16 size.

1 2. The method of claim 1, further comprising the steps of:

2 testing the width indication bit in the first stack save area in memory;
3 reading the data values and the least significant portion of the stack pointer value from the
4 first stack save area, and storing the data values into the least significant portions of the registers
5 and storing the least significant portion of the stack pointer value into the stack pointer register, and
6 clearing the most significant bit of the stack pointer register to indicate that the data values for the

7 procedure have the first word size if the width indication bit in the first stack save area in memory
8 does not indicate that the data values for the procedure have the second word size;

9 reading the data values and the stack pointer value from the second stack save area, and
10 storing the data values into the registers and storing the stack pointer value in the stack pointer
11 register if the width indication bit in the first stack save area in memory indicates that the data
12 values for the procedure have the second word size.

1 3. The method of claim 2, wherein the width indication bit in the first stack save area
2 comprises a least significant bit in a location of the first stack save area allocated to the stack
3 pointer value for the procedure.

1 4. The method of claim 2, wherein the first stack save area is specified by the stack
2 pointer value in the stack pointer register.

1 5. The method of claim 4, wherein the second stack save area is specified by the stack
2 pointer value in the stack pointer register plus an offset value that corresponds to an area in
3 memory required for the first stack save area.

1 6. The method of claim 5, wherein the first word size comprises 32 bits and the
2 second word size comprises 64 bits.

1 7. The method of claim 6, wherein the registers in the processor and the stack pointer
2 register in the processor comprise 16 registers each comprising 64 bits.

1 8. The method of claim 7, wherein the offset value and the area in memory for the first
2 stack save area each comprise 16 multiplied by 4 bytes per register.

1 9. A processor that executes procedures having differing word sizes, comprising:
2 means for testing a most significant bit of a stack pointer register in the processor that
3 indicates whether a set of data values for a procedure that are stored in a set of registers in the
4 processor each have a first word size or a second word size wherein the first word size is less than
5 the second word size;

6 means for transferring the data values from a least significant portion of each register to a
7 first stack save area in memory and transferring a least significant portion of a stack pointer value
8 from the stack pointer register to the first stack save area in memory if the most significant bit of
9 the stack pointer register indicates the first word size;

10 means for setting a width indication bit in the first stack save area in memory, and
11 transferring the data values from the registers to a second stack save area in memory and
12 transferring the stack pointer value from the stack pointer register to the second stack save area if
13 the most significant bit of the stack pointer register indicates the second word size such that the
14 width indication bit in the first stack save area in memory indicates that the data values for the
15 procedure have the second word size.

1 10. The processor of claim 9, further comprising:

2 means for testing the width indication bit in the first stack save area in memory;

3 means for reading the data values and the least significant portion of the stack pointer value
4 from the first stack save area, and storing the data values into the least significant portions of the
5 registers and storing the least significant portion of the stack pointer value into the stack pointer
6 register, and clearing the most significant bit of the stack pointer register to indicate that the data
7 values for the procedure have the first word size if the width indication bit in the first stack save
8 area in memory does not indicate that the data values for the procedure have the second word size;

9 means for reading the data values and the stack pointer value from the second stack save
10 area, and storing the data values into the registers and storing the stack pointer value in the stack

11 pointer register if the width indication bit in the first stack save area in memory indicates that the
12 data values for the procedure have the second word size.

1 11. The processor of claim 10, wherein the width indication bit in the first stack save
2 area comprises a least significant bit in a location of the first stack save area allocated to the stack
3 pointer value for the procedure.

1 12. The processor of claim 10, wherein the first stack save area is specified by the stack
2 pointer value in the stack pointer register.

1 13. The processor of claim 12, wherein the second stack save area is specified by the
2 stack pointer value in the stack pointer register plus an offset value that corresponds to an area in
3 memory required for the first stack save area.

1 14. The processor of claim 13, wherein the first word size comprises 32 bits and the
2 second word size comprises 64 bits.

1 15. The processor of claim 14, wherein the registers in the processor and the stack
2 pointer register in the processor comprise 16 registers each comprising 64 bits.

1 16. The processor of claim 15, wherein the offset value and the area in memory for the
2 first stack save area each comprise 16 multiplied by 4 bytes per register.

1 17. A method for context switching a processor that executes procedures having
2 differing word sizes, comprising the steps of:
3 testing a least significant bit of a stack pointer register in the processor that indicates
4 whether a set of data values for a procedure that are stored in a set of registers in the processor each

5 have a first word size or a second word size wherein the first word size is less than the second
6 word size;

7 transferring the data values from a least significant portion of each register to a first stack
8 save area in memory and transferring a least significant portion of a stack pointer value from the
9 stack pointer register to the first stack save area in memory if the least significant bit of the stack
10 pointer register indicates the first word size;

11 setting a width indication bit in the first stack save area in memory, and transferring the data
12 values from the registers to a second stack save area in memory and transferring the stack pointer
13 value from the stack pointer register to the second stack save area if the least significant bit of the
14 stack pointer register indicates the second word size such that the width indication bit in the first
15 stack save area in memory indicates that the data values for the procedure have the second word
16 size.

1 18. The method of claim 17, further comprising the steps of:

2 testing the width indication bit in the first stack save area in memory;

3 reading the data values and the least significant portion of the stack pointer value from the
4 first stack save area, and storing the data values into the least significant portions of the registers
5 and storing the least significant portion of the stack pointer value into the stack pointer register, and
6 clearing the least significant bit of the stack pointer register to indicate that the data values for the
7 procedure have the first word size if the width indication bit in the first stack save area in memory
8 does not indicate that the data values for the procedure have the second word size;

9 reading the data values and the stack pointer value from the second stack save area, and
10 storing the data values into the registers and storing the stack pointer value in the stack pointer
11 register if the width indication bit in the first stack save area in memory indicates that the data
12 values for the procedure have the second word size.

1 19. The method of claim 18, wherein the width indication bit in the first stack save area
2 comprises a least significant bit in a location of the first stack save area allocated to the stack pointer
3 value for the procedure.

1 20. The method of claim 18, wherein the first stack save area is specified by the stack
2 pointer value in the stack pointer register.

1 21. The method of claim 20, wherein the second stack save area is specified by the
2 stack pointer value in the stack pointer register plus an offset value that corresponds to an area in
3 memory required for the first stack save area.

1 22. The method of claim 21, wherein the first word size comprises 32 bits and the
2 second word size comprises 64 bits.

1 23. The method of claim 22, wherein the registers in the processor and the stack pointer
2 register in the processor comprise 16 registers each comprising 64 bits.

1 24. The method of claim 23, wherein the offset value and the area in memory for the
2 first stack save area each comprise 16 multiplied by 4 bytes per register.

1 25. A processor that executes procedures having differing word sizes, comprising:
2 means for testing a least significant bit of a stack pointer register in the processor that
3 indicates whether a set of data values for a procedure that are stored in a set of registers in the
4 processor each have a first word size or a second word size wherein the first word size is less than
5 the second word size;

6 means for transferring the data values from a least significant portion of each register to a
7 first stack save area in memory and transferring a least significant portion of a stack pointer value

8 from the stack pointer register to the first stack save area in memory if the least significant bit of the
9 stack pointer register indicates the first word size;

10 means for setting a width indication bit in the first stack save area in memory, and
11 transferring the data values from the registers to a second stack save area in memory and
12 transferring the stack pointer value from the stack pointer register to the second stack save area if
13 the least significant bit of the stack pointer register indicates the second word size such that the
14 width indication bit in the first stack save area in memory indicates that the data values for the
15 procedure have the second word size.

1 26. The processor of claim 25, further comprising:

2 means for testing the width indication bit in the first stack save area in memory;
3 means for reading the data values and the least significant portion of the stack pointer value
4 from the first stack save area, and storing the data values into the least significant portions of the
5 registers and storing the least significant portion of the stack pointer value into the stack pointer
6 register, and clearing the least significant bit of the stack pointer register to indicate that the data
7 values for the procedure have the first word size if the width indication bit in the first stack save
8 area in memory does not indicate that the data values for the procedure have the second word size;
9 means for reading the data values and the stack pointer value from the second stack save
10 area, and storing the data values into the registers and storing the stack pointer value in the stack
11 pointer register if the width indication bit in the first stack save area in memory indicates that the
12 data values for the procedure have the second word size.

1 27. The processor of claim 26, wherein the width indication bit in the first stack save
2 area comprises a least significant bit in a location of the first stack save area allocated to the stack
3 pointer value for the procedure.

1 28. The processor of claim 26, wherein the first stack save area is specified by the stack
2 pointer value in the stack pointer register.

1 29. The processor of claim 28, wherein the second stack save area is specified by the
2 stack pointer value in the stack pointer register plus an offset value that corresponds to an area in
3 memory required for the first stack save area.

1 30. The processor of claim 29, wherein the first word size comprises 32 bits and the
2 second word size comprises 64 bits.

1 31. The processor of claim 30, wherein the registers in the processor and the stack
2 pointer register in the processor comprise 16 registers each comprising 64 bits.

1 32. The processor of claim 31, wherein the offset value and the area in memory for the
2 first stack save area each comprise 16 multiplied by 4 bytes per register.

1 33. A method for context switching a processor that executes procedures having
2 differing word sizes, comprising the steps of:

3 testing a least significant bit of a stack pointer register in the processor that indicates
4 whether a set of data values for a procedure that are stored in a set of registers in the processor,
5 each have a first word size or a second word size, wherein the first word size is less than the
6 second word size;

7 transferring the data values from a least significant portion of each register to a first stack
8 save area in memory if the least significant bit of the stack pointer register indicates the first word
9 size;

10 transferring the data values from the registers to a second stack save area in memory if the
11 least significant bit of the stack pointer register indicates the second word size.

1 34. The method of claim 33, wherein the first stack save area is specified by a stack
2 pointer value in the stack pointer register.

1 35. The method of claim 34, wherein the second stack save area is specified by the
2 stack pointer value in the stack pointer register plus an offset value that corresponds to an area in
3 memory required for the first stack save area.

1 36. The method of claim 33, wherein the first word size comprises 32 bits and the
2 second word size comprises 64 bits.

1 37. The method of claim 33, wherein the registers in the processor and the stack pointer
2 register in the processor comprise 16 registers each comprising 64 bits.

1 38. The method of claim 35, wherein the offset value and the area in memory for the
2 first stack save area each comprise 16 multiplied by 4 bytes per register.